the semiconductor chip 1 is mounted on the wiring substrate 7 in face-down status. Connecting terminal (conductive bump) 4 being distributed over the entire area (for example, in an array shape) are formed on the formation surface 2 of the semiconductor element. The wiring substrate 7 comprises an insulated substrate main body 7A made of resin or the like, and a wiring layer (multi layer wiring) 7B is formed on the surface of the chip 1 side, the back surface and the inside of the wiring substrate 7. The bump 4 is arranged on the surface of the semiconductor element formation surface 2 side of the semiconductor chip 1 corresponding to the wiring layer 7B on the surface of the chip 1 side of the wiring substrate 7, and the semiconductor element formation surface 2 of the semiconductor chip 1 is electrically connected through the bump 4 to the wiring layer 7B of the wiring substrate 7. The wiring layer 7B on the surface of the chip 1 side of the wiring substrate 7 is also communicated to a wiring layer 7B arranged in the wiring substrate 7 and derived to the back surface side of the wiring substrate 7, and is electrically connected to a connecting terminal (conductive bump) 13 arranged on the back surface of the wiring substrate 7 for connection to a mother board.

IN THE CLAIMS:

Please amend claims 3, 19 and 20 as follows:

3. (Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a plurality of first connecting terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

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